Electronic Version
Stylesheet Version v1.1.1

Description

ADJUSTABLE IMPEDANCE CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an impedance circuit, and more specifically, to an adjustable impedance circuit whose equivalent impedance is determined by controlling the duty cycle of a control signal.

[0003] 2. Description of the Prior Art

[0004] There are two main problems when manufacturing a passive impedance device for an integrated circuit (IC).The first problem is concerned with the area occupied by large value passive impedance devices in an IC. For example, a resistor in an IC is often implemented by a metal line segment or polysilicon line segment, whose resistance is directly proportional to the length of the line segment. For another example, a capacitor in an IC is often implemented by a structure where a dielectric layer is inserted between two metal layers.The capacitance is directly pro-

portional to the area of the structure. The second problem is concerned with low precision of the passive impedance devices manufactured by semiconductor manufacturing process. Since many factors that cause errors exist in the manufacturing process, it is impossible to manufacture a passive impedance device with its value matching a theoretical value according to the requirements of circuit design. Take a resistor for example, even under the same manufacturing conditions, minute differencesbetween resistances exist. Therefore, the precision of the equivalent impedance value of a resistor is limited due to differencesin the manufacturing process. Especially if trying to manufacture two resistors ofa similar value (e.g. two resistors with resistancesof R and $R(1+e^{-6})$ respectively), the conventional semiconductor manufacturing process is not able to fulfill this requirement.

SUMMARY OF INVENTION

[0005] It is therefore a primary objective of the present invention to provide an adjustable impedance circuit whose equivalent impedance is determined by controlling the duty cycle of a control signal, in order to solve the problems mentioned above.

[0006] Briefly summarized, an impedance circuit for providing an

equivalent impedance between a first node and a second node includes a first impedance for providing a first impedance value, a first switch element electrically connected to the first impedance, a second impedance for providing a second impedance value, and a second switch element electrically connected to the second impedance. The equivalent impedance is determined by the first impedance value and the second impedance value, and by controlling the turn on time and the turn off time of the first switch element and the second switch element.

[0007] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0008] Fig.1 illustrates an adjustable impedance circuit according to the first embodiment of the present invention.

[0009] Fig.2 illustrates an adjustable impedance circuit according to the second embodiment of the present invention.

[0010] Fig.3 is a clock diagram of the first control signal and the second control signal.

[0011] Fig.4 is a flowchart of the operation of the adjustable

impedance circuit according to the present invention.

DETAILED DESCRIPTION

[0012] Please refer to Fig.1 showing an adjustable impedance circuit 40 according to the first embodiment of the present invention. In this embodiment, a first impedance 42 is formed by a resistor having a resistance of R_1, a second impedance 46 is formed by a resistor having a resistance of R_2, and a first switch element 44 includes a first switch 50 for being turned on and off according to a first control signal $CTRL_1$. In this embodiment, the first switch 50 is a transmission gate composed of an NMOS transistor and a PMOS transistor. The gate of the NMOS transistor is electrically connected to the first control signal $CTRL_1$, and the gate of the PMOS transistor is electrically connected to the first control signal $CTRL_1$ through an inverter in order toaccurately turn on and turn off the transmission gate. A second switch element 48 includes a third switch 52 for being turned on and off according to a second control signal $CTRL_2$. In this embodiment, the second switch 52 is also a transmission gate composed of an NMOS transistor and a PMOS transistor. The gate of the NMOS transistor is electrically connected to the second control signal $CTRL_2$, and the gate of the PMOS transistor

is electrically connected to the second control signal $CTRL_2$ through an inverter in order to accurately turn on and turn off the transmission gate. It should be noted that the first and the second switch 50, 52 can be NMOS or PMOS switch also.

[0013] Please refer to Fig.2 showing the adjustable impedance circuit 40 according to the second embodiment of the present invention. In this embodiment, the first switch element 44 further includes a second switch 58 electrically connected between a second node B and the other end of the first impedance 42, for being turned on and off according to the first control signal $CTRL_1$. And the second switch element 48 also includes a fourth switch 60 electrically connected between the second node B and the other end of the second impedance 46, for being turned on and off according to the second control signal $CTRL_2$.

[0014] In this embodiment, both the first switch 54 and the second switch 58 are NMOS transistors (as shown in Fig.2). The gates of these NMOS transistors are electrically connected to the first control signal $CTRL_1$ for being accuratelyturned on and off according to the first control signal $CTRL_1$. The third switch 56 and the fourth switch 60 are also MOS transistors (as shown in Fig.2). The gates of

these MOS transistors are electrically connected to the second control signal $CTRL_2$ for being accurately turned on and off according to the second control signal $CTRL_2$.

[0015] Please notice that although the first impedance 42 and the second impedance 46 are resistors in the embodiments mentioned above, they could also be other impedance devices such as capacitors and inductors. Additionally, although the first impedance 42 and the second impedance 46 in the embodiments mentioned above are implemented by at least one transmission gate or at least one MOS transistor, other devices which can achieve the same purpose also belong to the present invention.

[0016] The operation of the adjustable impedance circuit 40 disclosed by the second embodiment of the present invention is further described as follows. Please refer to Fig.3 showing a clock diagram of the first control signal $CTRL_1$ and the second control signal $CTRL_2$. In Fig.3, the first control signal $CTRL_1$ is a periodic signal with a period of Ttotal. The first control signal $CTRL_1$ is at the high level for a duration of T_1, that is, the duty cycle of the first control signal $CTRL_1$ is $DC_1=T_1/Ttotal$. The second control signal $CTRL_2$ is also a periodical signal with a period of Ttotal. The second control signal $CTRL_2$ is at the high level for a

duration of T_2, that is, the duty cycle of the second control signal $CTRL_2$ is $DC_2=T_2/Ttotal$. Since the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are used to turn on and off a plurality of NMOS transistors, both the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are active high signals.In other words, when the first control signal $CTRL_1$ and the second control signal $CTRL_2$areat a high level, the NMOS transistors are turned on. Please notice that in Fig.3, the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are complementary signals. However, this is not a strict requirement.The first control signal $CTRL_1$ and the second control signal $CTRL_2$ couldinstead be at a low level for a period of time.

[0017] As shown in Fig.3, between time t_0 and time t_1, since the first control signal $CTRL_1$ is ata high level and the second control signal $CTRL_2$ is at a low level, the first switch element 44 in Fig.2 is turned on so that the first impedance 42 is connected between a first node A and the second node B, and the second switch element 48 is turned off so that the second impedance 46 is not connected between the first node A and the second node B. Thus between time t_0 and time t_1, the impedance of the adjustable

impedance circuit 40 is equivalent to the resistance R_1. Between time t_1 and time t_2, since the first control signal $CTRL_1$ is at a low level and the second control signal $CTRL_2$ is at a high level, the first switch element 44 in Fig.2 is turned off so that the first impedance 42 is not connected between the first node A and the second node B, and the second switch element 48 is turned on so that the second impedance 46 is connected between a first node A and the second node B. Thus between time t_1 and time t_2, the impedance of the adjustable impedance circuit 40 is equivalent to the resistance R_2.

[0018] Please refer to Fig.4 showing a flowchart of the operation of the adjustable impedance circuit according to the present invention. The flowchart comprises the following steps:

[0019] Step10: Connect the first impedance to the second node.

[0020] Step12: Disconnect the first impedance from the second node.

[0021] Step14: Connect the second impedance to the first node and the second node.

[0022] Step16: Disconnect the second impedance from the sec-ond node.

[0023] It should be noted that the first impedance and the sec-

ond impedance are not necessarily alternatively connected or disconnected from the first node and the second node. They could also be connected and disconnected from the first node and the second node simultaneously.

[0024] As described above, if the time duration between time t_0 and time t_1 is T_1, and the time duration between time t_1 and time t_2 is T_2, when the first control signal $CTRL_1$ and the second control signal $CTRL_2$ switch periodically, the equivalent impedance Zeq between the first node A and the second node B can be represented by the following formula:

$$Zeq = \frac{T_1 R_1 + T_2 R_2}{T_{total}} = DC_1 R_1 + DC_2 R_2 \qquad \text{formula 1}$$

[0025] In this embodiment, since the first control signal $CTRL_1$

and the second control signal $CTRL_2$ are complimentary signals, $Ttotal=T_1+T_2$, and $DC_2=1-DC_1$. Substitute these equations into formula 1 to obtain formula 2 as follows:

$$Zeq = DC_1R_1 + (1 - DC_1)R_2 \qquad \text{formula 2}$$

[0026] For better performance, the frequencies of the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are often higher than the operating frequency of the adjustable impedance circuit 40 (e.g. a factor of ten higher).

[0027] If two resistors havingsimilar values are required in an IC, two adjustable impedance circuits 40 can be used (hereinafter referred as adjustable impedance circuit 40a and adjustable impedance circuit 40b). Assume that in the adjustable impedance circuits 40a and 40b, $R_1=2R_2$, and a very minute difference exists between the duty cycle DC_{1a}

of the first control signal $CTRL_1$ of the adjustable impedance circuit 40a and the duty cycle DC_{1b} of the first control signal $CTRL_1$ of the adjustable impedance circuit 40b (e.g. $DC_{1a}=(1+e^{-6})DC_{1b}$).The ratio of the equivalent impedance Zeqa of the adjustable impedance circuit 40a and the equivalent impedance Zeqb of the adjustable impedance circuit 40b can be obtained by the following formula:

$$\frac{Zeqa}{Zeqb}=\frac{(1+e^{-6})DC_{1b}\times 2R_2+(1-(1+e^{-6})DC_{1b})R_2}{DC_{1b}\times 2R_2+(1-DC_{1b})R_2}=1+\frac{e^{-6}}{1+\frac{1}{DC_{1b}}} \qquad \text{formula 3}$$

[0028] According to the result of formula 3, if the duty cycle DC_{1b} of the first control signal $CTRL_1$ of the adjustable impedance circuit 40b is 0.5, then $Reqa=(1+e^{-6}/3)Reqb$.

[0029] As described above, the adjustable impedance circuit 40

according to the present invention achieves the purpose of manufacturing two impedancesof very close values by the control of the first control signal $CTRL_1$ and the second control signal $CTRL_2$. Since thepresent circuit design technology precisely controls the features of digital signals (e.g. the duty cycle of the first control signal and the second control signal), the present invention solves the problem of the conventional art.

[0030] Please notice that, in the embodiments mentioned above, the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are implemented by complementary periodic signals as shown in Fig.3. However according to practical requirements, the first control signal $CTRL_1$ and the second control signal $CTRL_2$ can also control the adjustable impedance circuit 40 so that the first impedance 42 and the second impedance 46 are simultaneously connected between the first node A and the second node B during a specific time period. In this time period, the equivalent impedance between the first node A and the second node B equals the parallel impedance of the first impedance 42 and the second impedance 46. The first control signal $CTRL_1$ and the second control signal $CTRL_2$ can also control the adjustable impedance circuit 40 so that the first

impedance 42 and the second impedance 46 are simultaneously disconnected from the first node A and the second node B during a specific time period. In this time period, the first node A and the second node B are disconnected.

[0031] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.